Institute for High-Frequency & Communication Technology

Master-Thesis

FPGA implementation of compressed sensing algorithms

Nowadays all digital electronic devices employ a processor as the heart of the system. Field-programmable gate-arrays (FPGAs) are arrays of reconfigurable digital circuits and switches that can be programmed to perform specific functions, for example as a signal processor. Its advantage over CPUs it that they can be customized for a specific task and, thus, become more efficient than a general-purpose CPU. This capability becomes crucial for the implementation of sparse reconstruction algorithms in the framework of "compressed sensing" (CS). CS is a novel sampling theory that allows condensing the information of interest into a reduced set of samples, thus drastically reducing data storage and transmission needs. However, CS brings the need of dedicated algorithms to decode the signal, encoded in few measurements. In this thesis, the power of FPGAs will be unleashed to provide an efficient algorithmic counterpart, allowing real-time reconstruction of 2D and 3D data from compressed measurements.

Requirements:

- Logic circuit theory
- familiarity with VHDL or Verilog
- proficiency in MATLAB or python
- basic knowledge of communications theory and/or signal processing is an advantage
- moderate English

After this thesis, there are good career prospects in the following areas:

- Digital hardware design
- Signal processing
- 2D/3D sensing

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